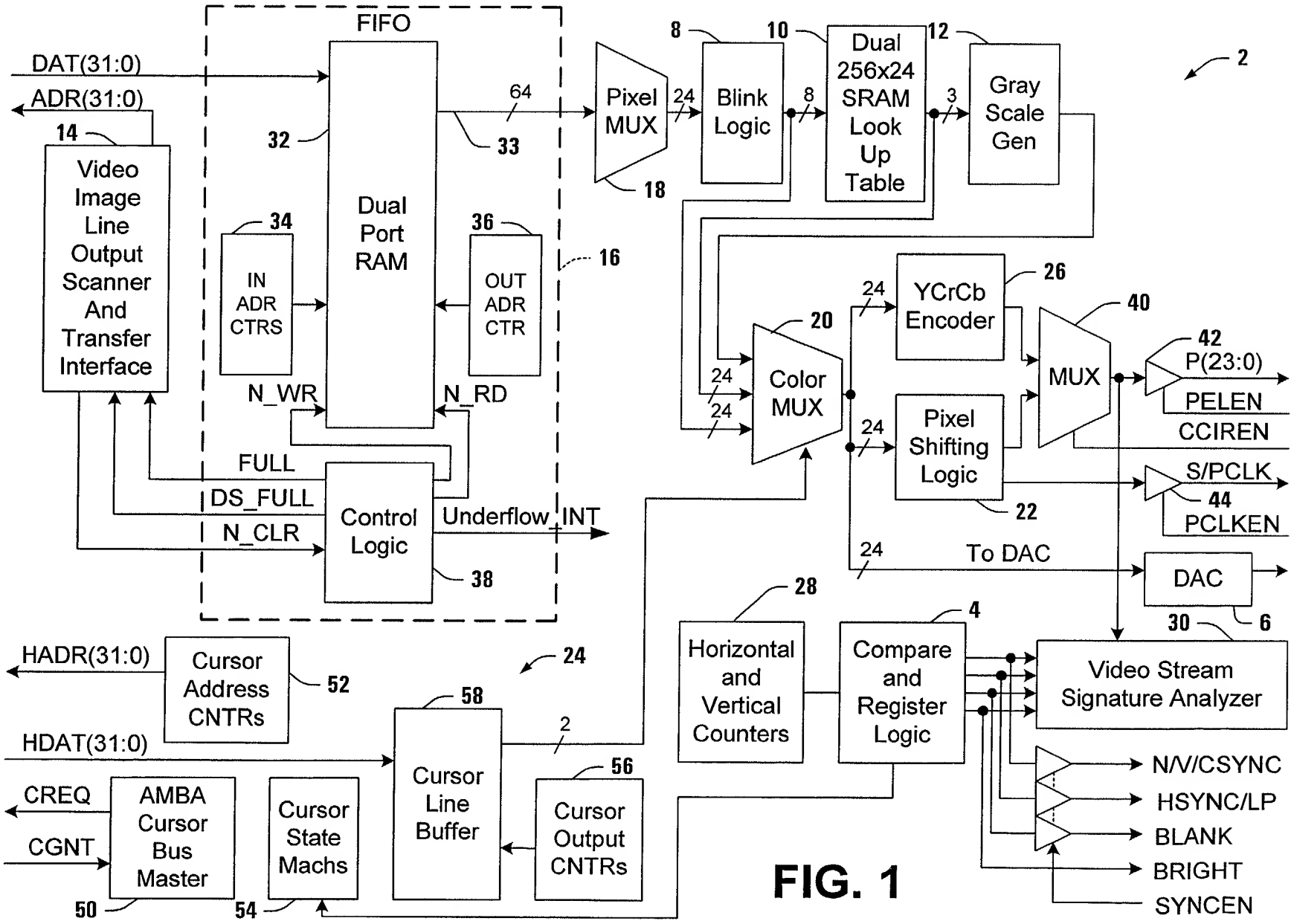
FIFO
DAT(31:0)
ADR(31:0)
14
Video Image Line Output Scanner And Transfer Interface
32
Dual Port RAM
64
33
Pixel MUX
24
18
8
Blink Logic
10
Dual 256x24 SRAM Look Up Table
12
3
Gray Scale Gen
2
16
34
IN ADR CTRS
36
OUT ADR CTR
N_WR
N_RD
FULL
DS_FULL
N_CLR
Control Logic
Underflow
INT
38
20
Color MUX
24
YCrCb Encoder
26
40
MUX
42
P(23:0)
PELEN
CCIREN
Pixel Shifting Logic
22
S/PCLK
44
PCLKEN
To DAC
DAC
30
6
28
Horizontal and Vertical Counters
4
Compare and Register Logic
Video Stream Signature Analyzer
N/V/CSYNC
HSYNC/LP
BLANK
BRIGHT
SYNCEN
24
HADR(31:0)
Cursor Address CNTRs
52
58
2
HDAT(31:0)
Cursor Line Buffer
56
Cursor Output CNTRs
CREQ
CGNT
AMBA Cursor Bus Master
50
Cursor State Machs
54

FIG. 1

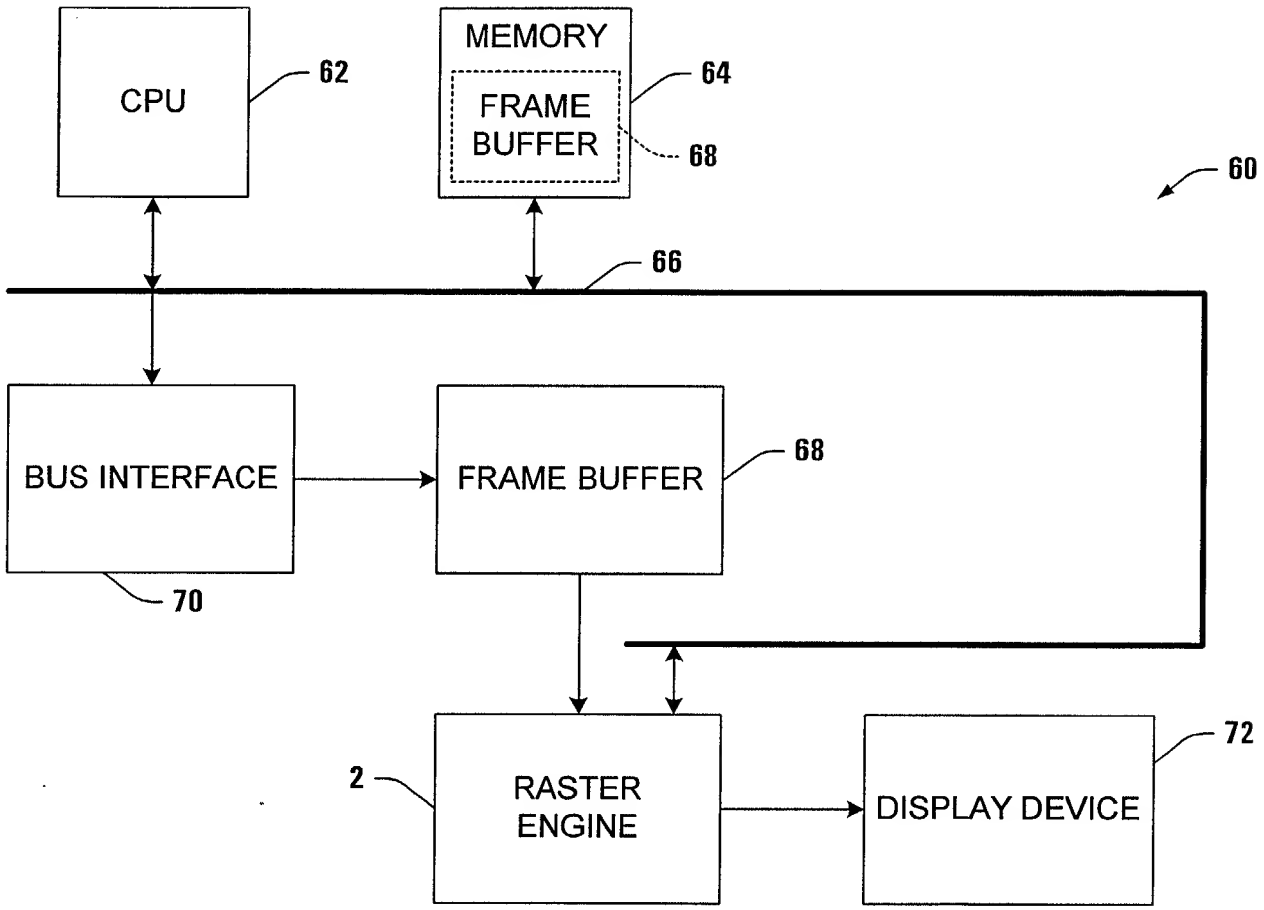
CPU
62
MEMORY
FRAME BUFFER
64
68
60
66
BUS INTERFACE
FRAME BUFFER
68
70
2
RASTER ENGINE
DISPLAY DEVICE
72

FIG. 2A

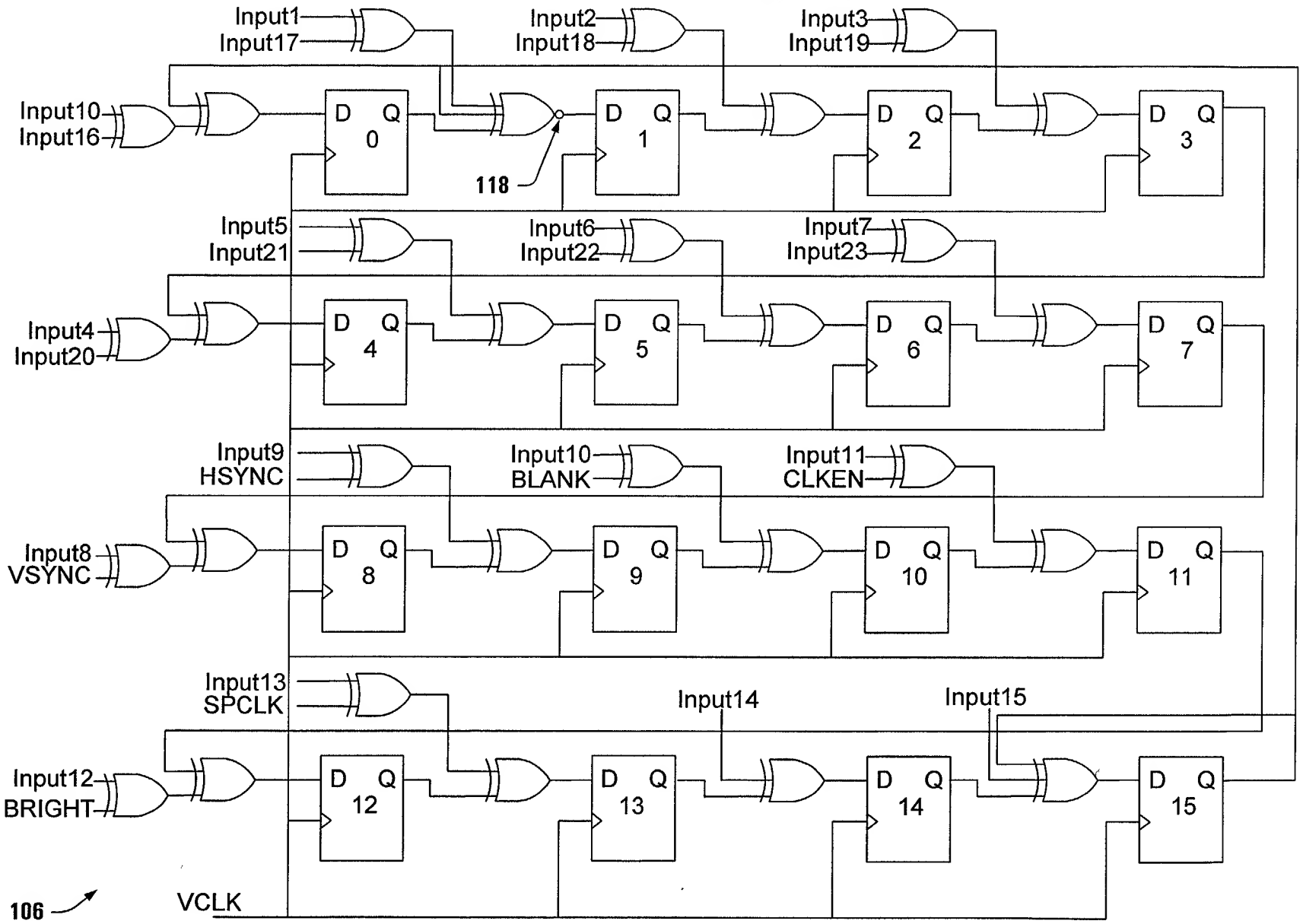
Input1
Input17
Input2
Input18
Input3
Input19
Input10
Input16
D Q
0
1
2
3
118
Input5
Input21
Input6
Input22
Input7
Input23
Input4
Input20
4
5
6
7
Input9
HSYNC
Input10
BLANK
Input11
CLKEN
Input8
VSYNC
8
9
10
11
Input13
SPCLK
Input14
Input15
Input12
BRIGHT
12
13
14
15
106
VCLK

FIG. 4

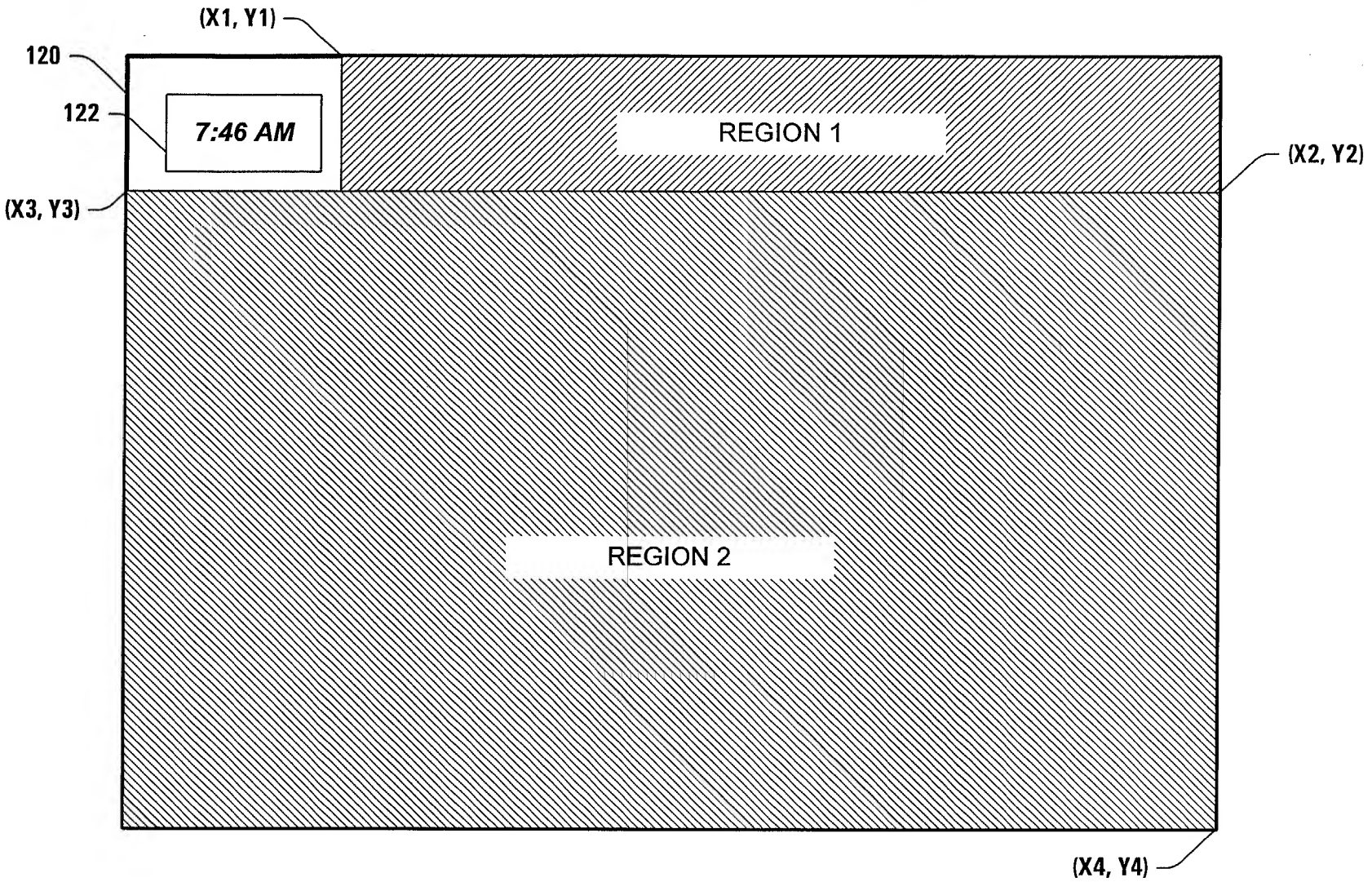

FIG. 5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RSVD	SPCLK	BRIGHT	CLKEN	BLANK	HSYNC	VSYNC	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN

SIGCTL

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FIG. 6B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	STOP 10	STOP 9	STOP 8	STOP 7	STOP 6	STOP 5	STOP 4	STOP 3	STOP 2	STOP 1	STOP 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	START 10	START 9	START 8	START 7	START 6	START 5	START 4	START 3	START 2	START 1	START 0

VSIGSTRTSTOP

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FIG. 6C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	STOP 10	STOP 9	STOP 8	STOP 7	STOP 6	STOP 5	STOP 4	STOP 3	STOP 2	STOP 1	STOP 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	START 10	START 9	START 8	START 7	START 6	START 5	START 4	START 3	START 2	START 1	START 0

HSIGSTRTSTOP

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FIG. 6D

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	VCLR 10	VCLR 9	VCLR 8	VCLR 7	VCLR 6	VCLR 5	VCLR 4	VCLR 3	VCLR 2	VCLR 1	VCLR 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	HCLR 10	HCLR 9	HCLR 8	HCLR 7	HCLR 6	HCLR 5	HCLR 4	HCLR 3	HCLR 2	HCLR 1	HCLR 0

SIGCLR

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FIG. 6E

Patent Application

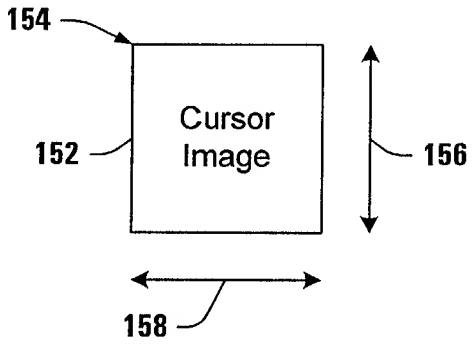

FIG. 7A

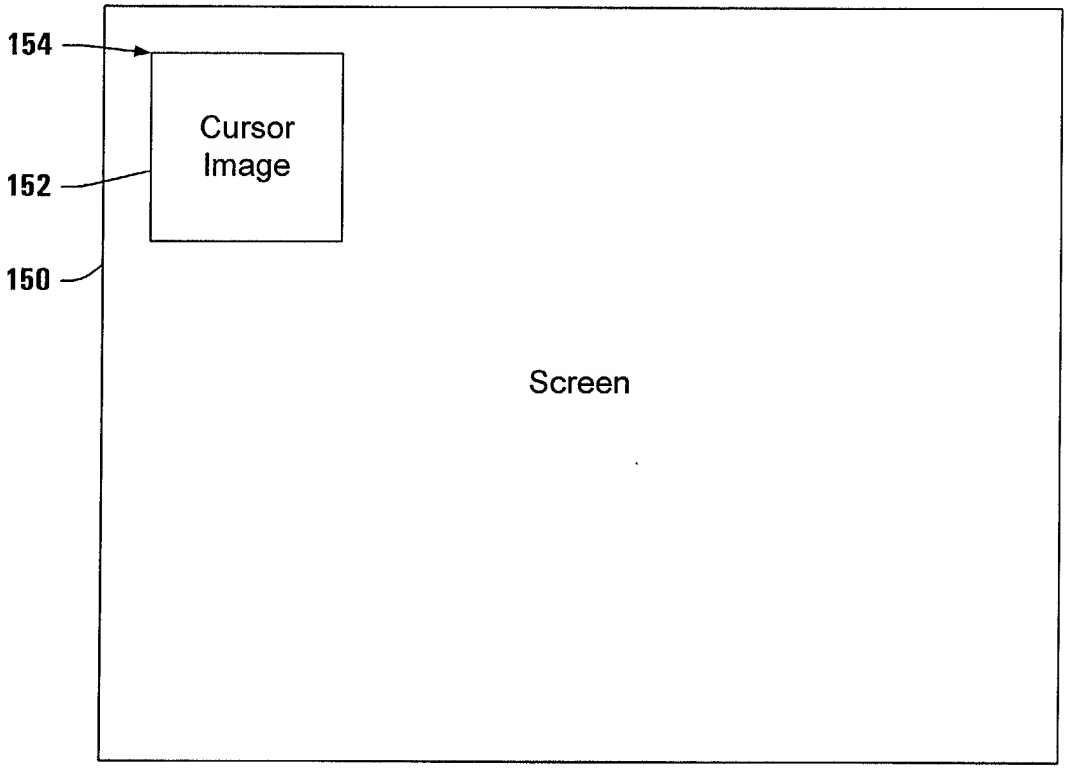

FIG. 7B

Test Image

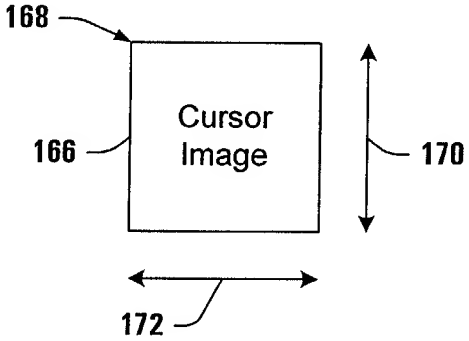

FIG. 8A

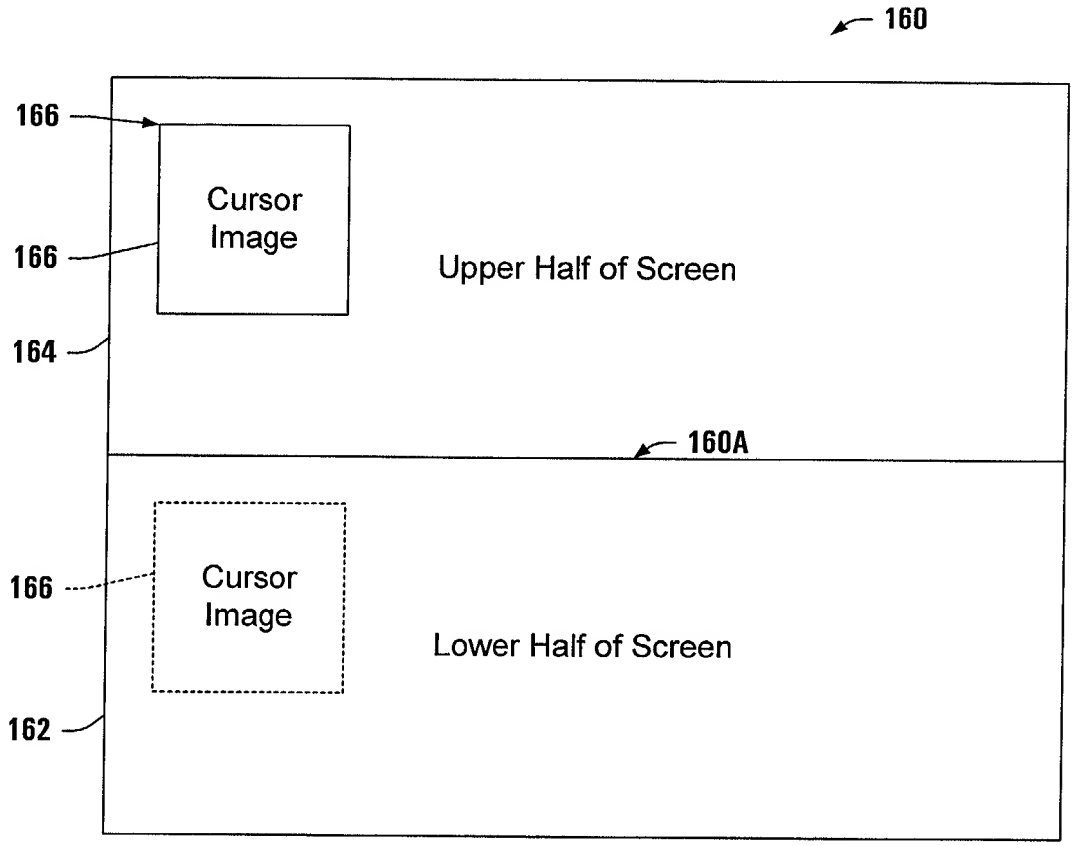

FIG. 8B

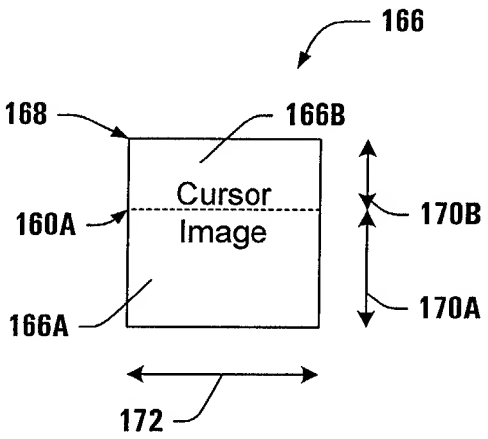
166
168
166B
Cursor
Image
160A
170B
170A
166A
172

FIG. 9A

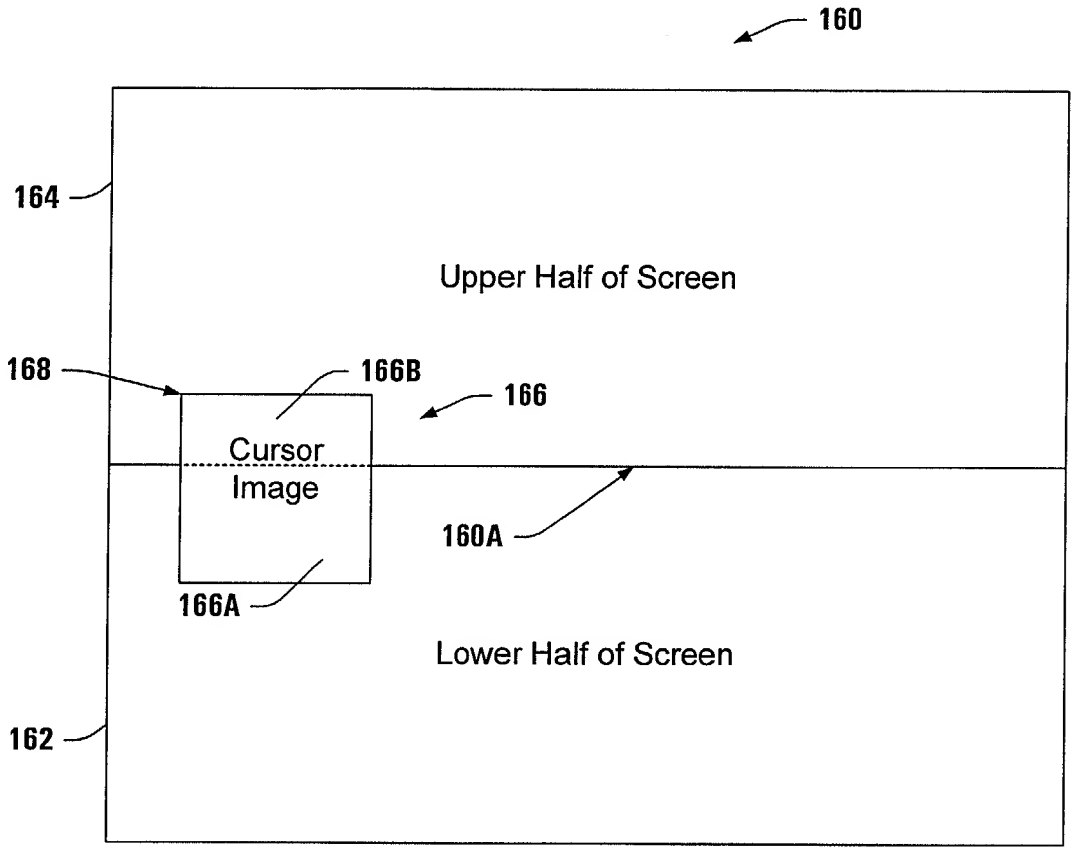
160
164
Upper Half of Screen
168
166B
166
Cursor
Image
160A
166A
Lower Half of Screen
162

FIG. 9B

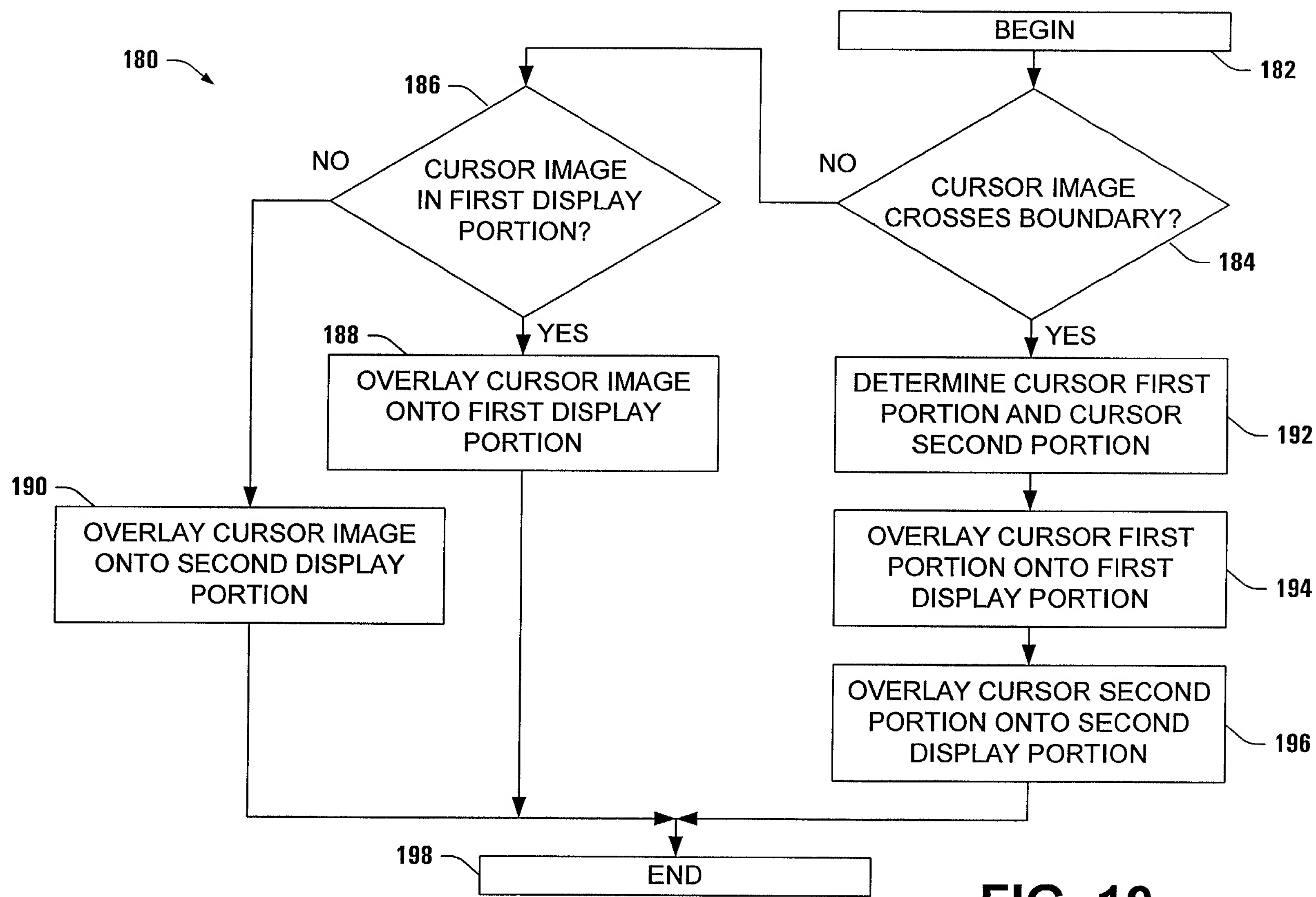
180
BEGIN
182
CURSOR IMAGE CROSSES BOUNDARY?
184
NO
YES
DETERMINE CURSOR FIRST PORTION AND CURSOR SECOND PORTION
192
OVERLAY CURSOR FIRST PORTION ONTO FIRST DISPLAY PORTION
194
OVERLAY CURSOR SECOND PORTION ONTO SECOND DISPLAY PORTION
196
186
CURSOR IMAGE IN FIRST DISPLAY PORTION?
NO
YES
188
OVERLAY CURSOR IMAGE ONTO FIRST DISPLAY PORTION
190
OVERLAY CURSOR IMAGE ONTO SECOND DISPLAY PORTION
198
END

FIG. 10

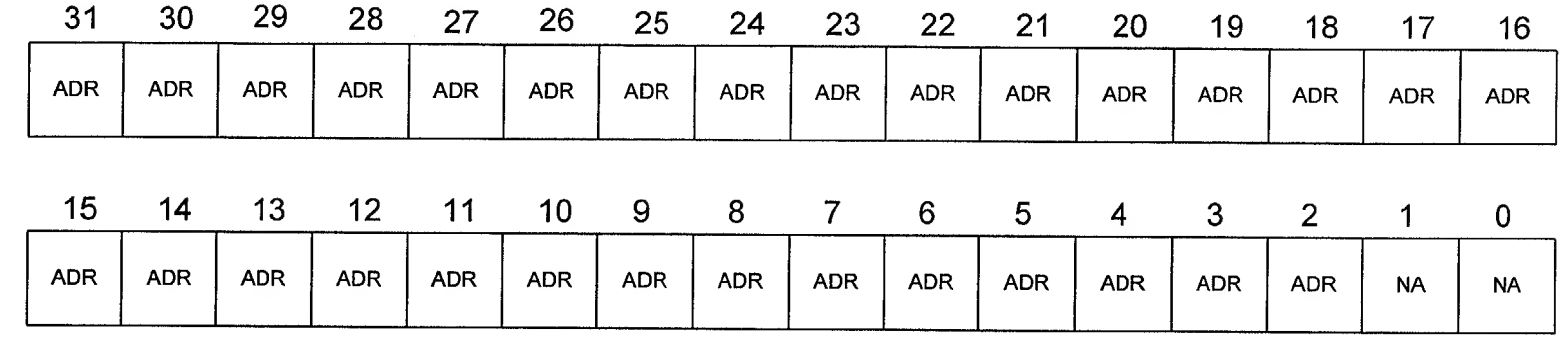

FIG. 11A

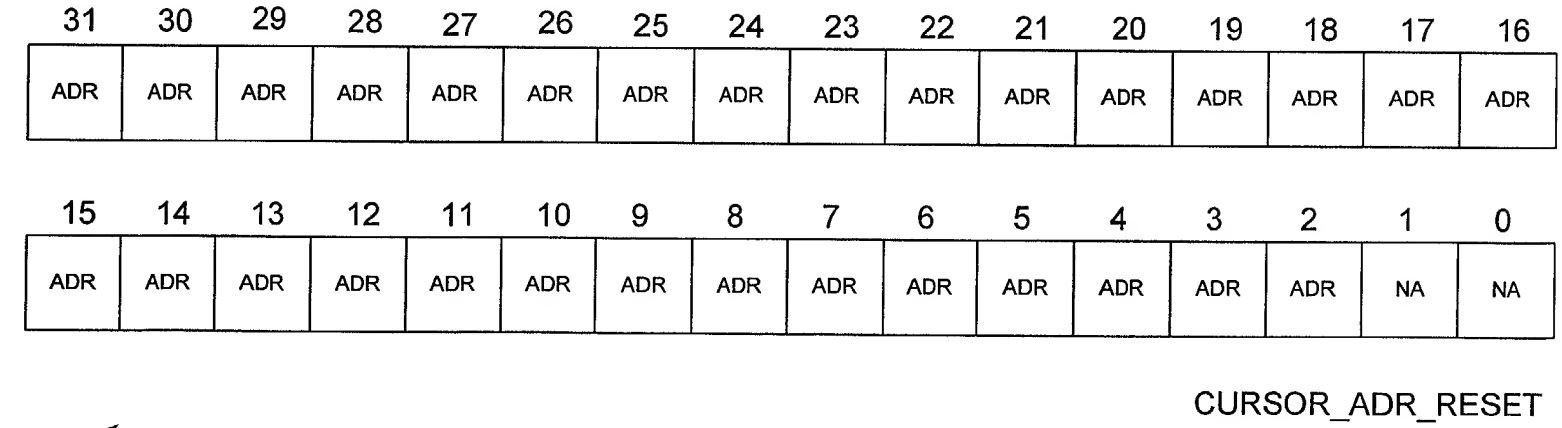

FIG. 11B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLNS5	DLNS4	DLNS3	DLNS2	DLNS1	DLNS0	CSTEP 1	CSTEP 0	CLINS5	CLINS4	CLINS3	CLINS2	CLINS1	CLINS0	CWID1	CWID0

CURSORSIZE

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FIG. 11C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R	COLO R

CURSORCOLOR1
CURSORCOLOR2
CURSORBLINK1
CURSORBLINK2

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FIG. 11D

Patent Application

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	YLOC 10	YLOC 9	YLOC 8	YLOC 7	YLOC 6	YLOC 5	YLOC 4	YLOC 3	YLOC 2	YLOC 1	YLOC 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CEN	RSVD	RSVD	RSVD	RSVD	XLOC 10	XLOC 9	XLOC 8	XLOC 7	XLOC 6	XLOC 5	XLOC 4	XLOC 3	XLOC 2	XLOC 1	XLOC 0

CURSORXYLOC

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FIG. 11E

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLHEN	RSVD	RSVD	RSVD	RSVD	YLOC 10	YLOC 9	YLOC 8	YLOC 7	YLOC 6	YLOC 5	YLOC 4	YLOC 3	YLOC 2	YLOC 1	YLOC 0

CURSOR_DHSCAN_LH_YLOC

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FIG. 11F

Patent Application Publication

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EN	RATE	RATE	RATE	RATE	RATE	RATE	RATE	RATE

CURSORBLINK

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FIG. 11G

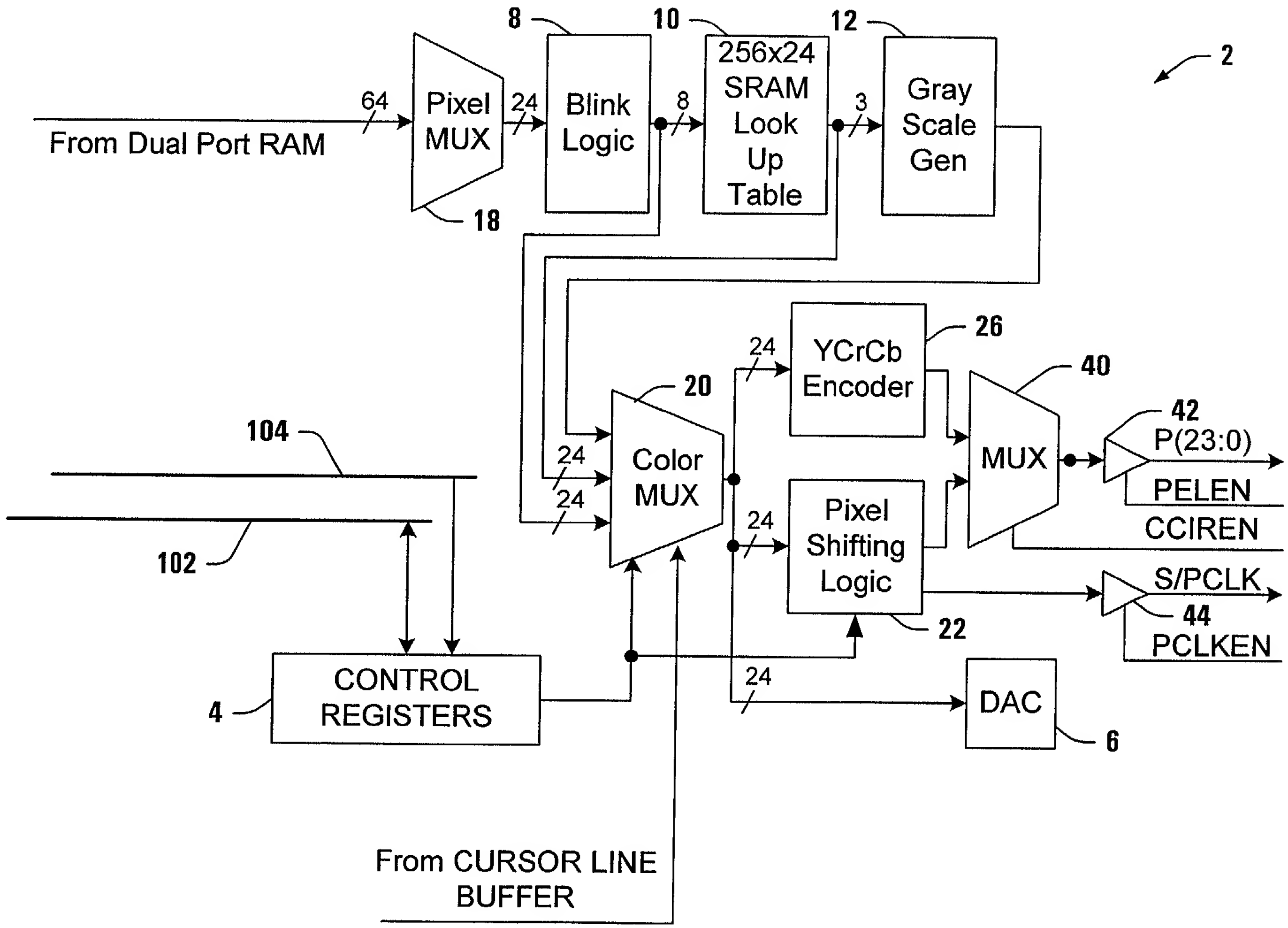
2
From Dual Port RAM
64
Pixel MUX
18
24
8
Blink Logic
10
8
256x24 SRAM Look Up Table
12
3
Gray Scale Gen
104
102
20
24
24
Color MUX
24
YCrCb Encoder
26
24
Pixel Shifting Logic
22
40
MUX
42
P(23:0)
PELEN
CCIREN
S/PCLK
44
PCLKEN
4
CONTROL REGISTERS
24
DAC
6
From CURSOR LINE BUFFER

FIG. 12

TESTING EMBEDDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	DSCA	C3	C2	C1	C0	M3	M2	M1	M0	S2	S1	S0	P2	P1	P0

PIXELMODE

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FIG. 13A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RD	DAT	DAT	DAT	DAT	DAT	DAT	DAT	DAT

PARLLIFOUT

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FIG. 13B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ESTR T3	ESTR T2	ESTR T1	ESTR T0	CNT3	CNT2	CNT1	CNT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	DAT	DAT	DAT	DAT	DAT	DAT	DAT	DAT

PARLLIFIN

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FIG. 13C

shift mode	color mode	output mode	P(23) ***	P(22) ***	P(21) ***	P(20) ***	P(19) ***	P(18) ***	P(17)	P(16)	P(15)	P(14)	P(13) ****	P(12)	P(11)	P(10)	P(9) ****	P(8)	P(7)	P(6)	P(5) ****	P(4)	P(3)	P(2)	P(1) ****	P(0)
0x0	0x0 0x4 0x8	single pixel per clock up to 24 bits wide	R(1)	R(0)	G(1)	G(0)	B(1)	B(0)	R(7)	R(6)	R(5)	R(4)	R(3)	R(2)	G(7)	G(6)	G(5)	G(4)	G(3)	G(2)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)
0x0	0x5	single 16-bit 565 pixel per clock	R(3)	R(2)	G(5)	G(4)	B(3)	B(2)	R(4)	R(3)	R(2)	R(1)	R(0)	R(4)	G(5)	G(4)	G(3)	G(2)	G(1)	G(0)	B(4)	B(3)	B(2)	B(1)	B(0)	B(4)
0x0	0x6	single 16-bit 555 pixel per clock	R(3)	R(2)	G(3)	G(2)	B(3)	P(2)	R(4)	R(3)	R(2)	R(1)	R(0)	R(4)	G(4)	G(3)	G(2)	G(1)	G(0)	G(4)	B(4)	B(3)	B(2)	B(1)	B(0)	B(4)
0x1	0x0 0x4 0x8	single 24 bit pixel mapped to 18 bits each clk	X	X	X	X	X	X	R(7)	R(6)	R(5)	R(4)	R(3)	R(2) *	G(7)	G(6)	G(5)	G(4)	G(3)	G(2) *	B(7)	B(6)	B(5)	B(4)	B(3)	B(2) *
0x1	0x5	single 16-bit 565 pixel mapped to 18 bits each clk	X	X	X	X	X	X	R(4)	R(3)	R(2)	R(1)	R(0)	R(4) *	G(5)	G(4)	G(3)	G(2)	G(1)	G(0) *	B(4)	B(3)	B(2)	B(1)	B(0)	B(4) *
0x1	0x6	single 16-bit 555 pixel mapped to 18 bits each clk	X	X	X	X	X	X	R(4)	R(3)	R(2)	R(1)	R(0)	R(4) *	G(4)	G(3)	G(2)	G(1)	G(0)	G(4) *	B(4)	B(3)	B(2)	B(1)	B(0)	B(4) *
0x2	0x0 0x8	progressive scan 2 pixels per shift clock dual scan	P1(20) R1(4) *	P1(12) G1(4) *	P1(4) B1(4) *	P0(20) R0(4) *	P0(12) G0(4) *	P0(4) B0(4) *	P1(23) R1(7)	P1(22) G1(6)	P1(21) G1(5)	P1(15) G1(7)	P1(14) G1(6)	P1(13) G1(5)	P1(7) B1(7)	P1(6) B1(6)	P1(5) B1(5)	P0(23) R0(7)	P0(22) R0(6)	P0(21) R0(5)	P0(15) G0(7)	P0(14) G0(6)	P0(13) G0(5)	P0(7) B0(7)	P0(6) B0(6)	P0(5) B0(5)
			Lower P(20) R(4) *	Lower P(12) G(4) *	Lower P(4) B(4) *	Upper P(20) R(4) *	Upper P(12) G(4) *	Upper P(4) B(4) *	Lower P(23) R(7)	Lower P(22) R(6)	Lower P(21) R(5)	Lower P(15) G(7)	Lower P(14) G(6)	Lower P(13) G(5)	Lower P(7) B(7)	Lower P(6) B(6)	Lower P(5) B(5)	Upper P(23) R(7)	Upper P(22) R(6)	Upper P(21) R(5)	Upper P(15) G(7)	Upper P(14) G(6)	Upper P(13) G(5)	Upper P(7) B(7)	Upper P(6) B(6)	Upper P(5) B(5)
0x3	0x0 0x8	progressive scan 4 pixels per shift clock dual scan	P3(14) G3(6) *	P3(6) B3(6) *	P2(14) B2(6) *	P2(6) B2(6) *	P1(14) G1(6) *	P1(6) B1(6) *	P0(14) G0(6) *	P0(6) B0(6) *	P3(23) R3(7)	P3(22) R3(6) *	P3(15) G3(7)	P3(7) B3(7)	P2(23) R2(7)	P2(22) R2(6) *	P2(15) G2(7)	P2(7) B2(7)	P1(23) R1(7)	P1(22) R1(6) *	P1(15) G1(7)	P1(7) B1(7)	P0(23) R0(7)	P0(22) R0(6) *	P0(15) G0(7)	P0(7) B0(7)
			Lower P1(14) G1(6) *	Lower P1(6) B1(6) *	Upper P1(14) G1(6) *	Upper P1(6) B1(6) *	Lower P0(14) G0(6) *	Lower P0(6) B0(6) *	Upper P0(14) G0(6) *	Upper P0(6) B0(6) *	Lower P1(23) R1(7)	Lower P1(22) R1(6) *	Lower P1(15) G1(7)	Lower P1(7) B1(7)	Upper P1(23) R1(7)	Upper P1(22) R1(6) *	Upper P1(15) G1(7)	Upper P1(7) B1(7)	Lower P0(23) R0(7)	Lower P0(22) R0(6) *	Lower P0(15) G0(7)	Lower P0(7) B0(7)	Upper P0(23) R0(7)	Upper P0(22) R0(6) *	Upper P0(15) G0(7)	Upper P0(7) B0(7)

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FIG. 14A

PATENT CLASSES

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0x4	0x0 0x8	progressive scan **8 pixels per shift clock** dual scan	P7(23) R7 *	P6(23) R6 *	P5(23) R5 *	P4(23) R4 *	P3(23) R3 *	P2(23) R2 *	P1(23) R1 *	P0(23) R0 *	P7(15) G7 *	P7(7) B7 *	P6(15) G6 *	P6(7) B6 *	P5(15) G5 *	P5(7) B5 *	P4(15) G4 *	P4(7) B4 *	P3(15) G3 *	P3(7) B3 *	P2(15) G2 *	P2(7) B2 *	P1(15) G1 *	P1(7) B1 *	P0(15) G0 *	P0(7) B0 *
			Lower P3(23) R3 *	Upper P3(23) R3 *	Lower P2(23) R2 *	Upper P2(23) R2 *	Lower P1(23) R1 *	Upper P1(23) R1 *	Lower P0(23) R0 *	Upper P0(23) R0 *	Lower P3(15) G3 *	Lower P3(7) B3 *	Upper P3(15) G3 *	Upper P3(7) B3 *	Lower P2(15) G2 *	Lower P2(7) B2 *	Upper P2(15) G2 *	Upper P2(7) B2 *	Lower P1(15) G1 *	Lower P1(7) B1 *	Upper P1(15) G1 *	Upper P1(7) B1 *	Lower P0(15) G0 *	Lower P0(7) B0 *	Upper P0(15) G0 *	Upper P0(7) B0 *
0x5	0x0 0x8	**2 2/3 pixels per clock**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	G2	B2	R1	G1	B1	R0	G0	B0
			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B5	R4	G4	B4	R3	G3	B3	R2
			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R7	G7	B7	R6	G6	B6	R5	G5
0x6	0x0 0x8	**Dual 2 2/3 pixels per clock**	X	X	X	X	X	X	X	X	L G2	L B2	L R1	L G1	L B1	L R0	L G0	L B0	U G2	U B2	U R1	U G1	U B1	U R0	U G0	U B0
			X	X	X	X	X	X	X	X	L B5	L R4	L G4	L B4	L R3	L G3	L B3	L R2	U B5	U R4	U G4	U B4	U R3	U G3	U B3	U R2
			X	X	X	X	X	X	X	X	L R7	L G7	L B7	L R6	L G6	L B6	L R5	L G5	U R7	U G7	U B7	U R6	U G6	U B6	U R5	U G5
**	**	**CCIREN subs**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	D(7)	D(6)	D(5)	D(4)	D(3)	D(2)	D(1)	D(0)
**	**	**LCDEN subs**	**	**	**	**	**	**	**	XECL	YSCL	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**
**	**	**ACEN subs**	**	**	**	**	**	**	AC	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**

* These bits are an ORed combination of the bit value shown and the next significant bit below (This rounds the color value to nearest color)
** These bits do not get a substitute and are defined to the values controlled by the pixel output mode in the upper part of the table

*** These bits are pinned out in CL-EP9215 Dillon II only They are the MSBs of the color channels

**** Set PIXELMODE P13951 high to use these pins as outputs in the CL-EP9209

FIG. 14B

PATENT APPLICATION

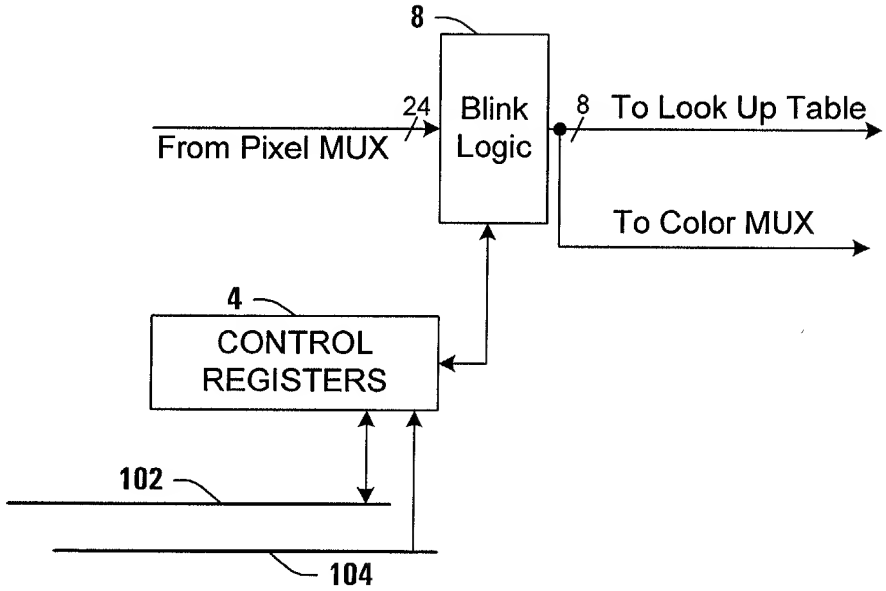

FIG. 15

Patent Application

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RATE	RATE	RATE	RATE	RATE	RATE	RATE	RATE

BLINKRATE

250

FIG. 16A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK	MASK

BLINKMASK

252

FIG. 16B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN	PATRN

BLINKPATRN

254

FIG. 16C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK	P MASK

PATTERNMASK

256

FIG. 16D

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF	BGOFF

BG_OFFSET

258

FIG. 16E

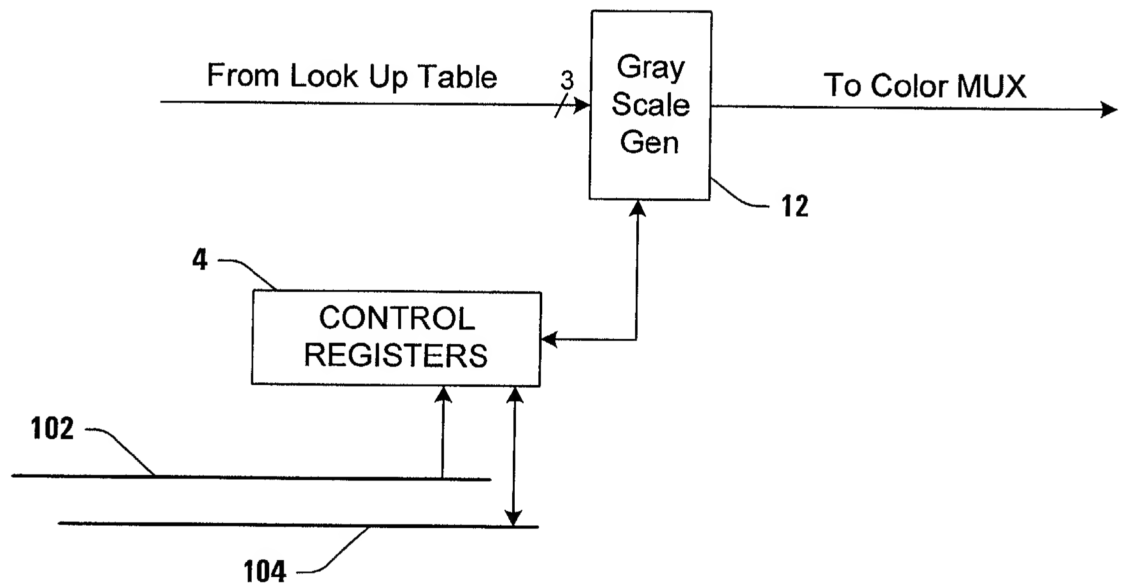
From Look Up Table
3
Gray Scale Gen
To Color MUX
12
4
CONTROL REGISTERS
102
104

FIG. 17

POSITA CLOSED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FRAME	VERT	HORZ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

GRAYSCALE LUT

282

FIG. 19

Patent Application

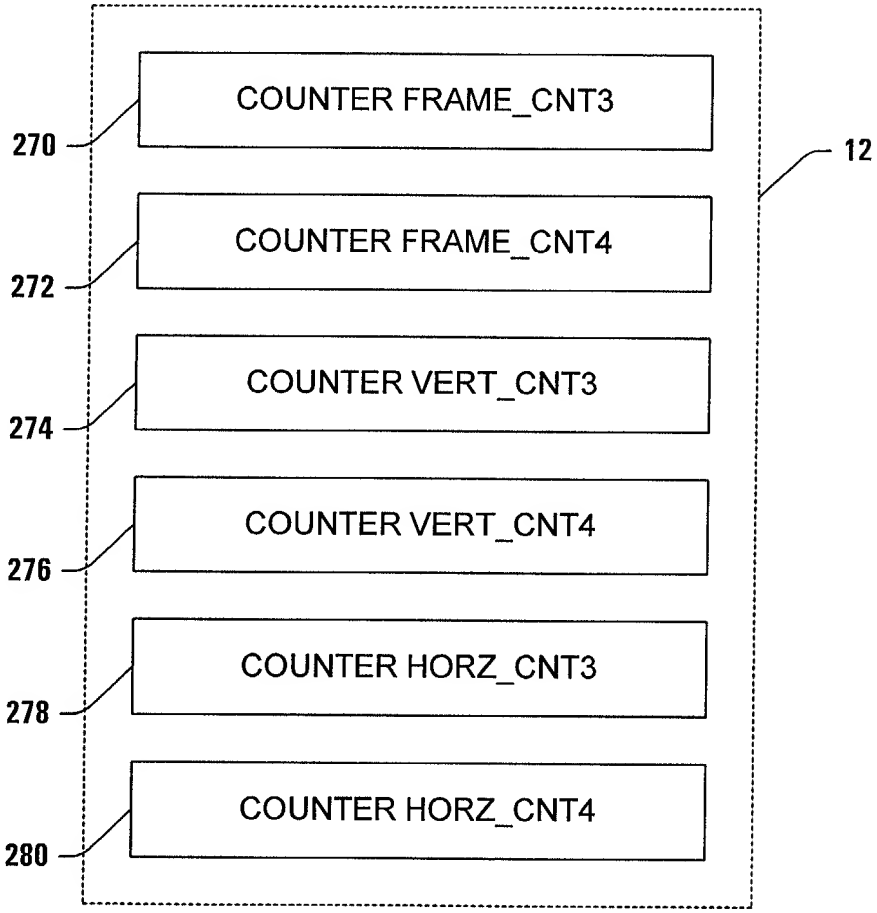

FIG. 18

F,V,H def	FRAME	Vert	Horz	VCNT (lines)	11	11	11	11	10	10	10	10	01	01	01	01	00	00	00	00	GSLUT Address *4	
for pixel	Ctr	Ctr	Ctr	HCNT (pixels)	11	10	01	00	11	10	01	00	11	10	01	00	11	10	01	00	FRAME	Pixel
in value				register address																		Value
000	D18	D17	D16	base + 0x80	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	000
001	D18	D17	D16	base + 0x84	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	001
010	D18	D17	D16	base + 0x88	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	010
011	D18	D17	D16	base + 0x8C	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	011
100	D18	D17	D16	base + 0x90	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	100
101	D18	D17	D16	base + 0x94	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	101
110	D18	D17	D16	base + 0x98	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	110
111	D18	D17	D16	base + 0x9C	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	00	111
	X	X	X	base + 0xA0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	000
	X	X	X	base + 0xA4	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	001
	X	X	X	base + 0xA8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	010
	X	X	X	base + 0xAC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	011
	X	X	X	base + 0xB0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	100
	X	X	X	base + 0xB4	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	101
	X	X	X	base + 0xB8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	110
	X	X	X	base + 0xBC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	01	111
	X	X	X	base + 0xC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	000
	X	X	X	base + 0xC4	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	001
	X	X	X	base + 0xC8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	010
	X	X	X	base + 0xCC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	011
	X	X	X	base + 0xD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	100
	X	X	X	base + 0xD4	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	101
	X	X	X	base + 0xD8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	110
	X	X	X	base + 0xDC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	10	111
	X	X	X	base + 0xE0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	000
	X	X	X	base + 0xE4	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	001
	X	X	X	base + 0xE8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	010
	X	X	X	base + 0xEC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	011
	X	X	X	base + 0xF0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	100
	X	X	X	base + 0xF4	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	101
	X	X	X	base + 0xF8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	110
	X	X	X	base + 0xFC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	11	111

300

FIG. 20

PATENT CLASSES

FRAME	Vert	Horz	VCNT (lines)	11	11	11	11	10	10	10	10	01	01	01	01	00	00	00	00	GSLUT Address *4	
Ctr	Ctr	Ctr	HCNT (pixels)	11	10	01	00	11	10	01	00	11	10	01	00	11	10	01	00	FRAME	Pixel
D18	D17	D16	register address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		Value
X	X	X	base + 0x80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00	000
			base + 0xA0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	01	000
			base + 0xC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10	000
			base + 0xE0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11	000
X	X	X	base + 0x9C	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	00	111
			base + 0xBC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	01	111
			base + 0xDC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	10	111
			base + 0xFC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	11	111

302

FIG. 21

304

FRAME 0

	H	O	R	Z
V	1	1	1	1
E	1	1	1	1
R	1	1	1	1
T	1	1	1	1

FRAME 1

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

FRAME 2

1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1

FRAME 3

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

FIG. 22

306

FRAME 0

	H	O	R	Z
V	1	0	1	0
E	1	0	1	0
R	1	0	1	0
T	1	0	1	0

FRAME 1

0	1	0	1
0	1	0	1
0	1	0	1
0	1	0	1

FRAME 2

1	0	1	0
1	0	1	0
1	0	1	0
1	0	1	0

FRAME 3

0	1	0	1
0	1	0	1
0	1	0	1
0	1	0	1

FIG. 23

TESTING ELEMENT

308

FRAME 0

	H	O	R	Z
V	1	1	0	0
E	1	0	1	0
R	0	0	1	1
T	1	0	1	0

FRAME 1

0	0	1	1
0	1	0	1
1	1	0	0
0	1	0	1

FRAME 2

1	0	1	0
1	1	0	0
1	0	1	0
0	0	1	1

FRAME 3

0	1	0	1
0	0	1	1
0	1	0	1
1	1	0	0

FIG. 24

FRAME	Vert	Horz	VCNT (lines)	11	11	11	11	10	10	10	10	01	01	01	01	00	00	00	00	GSLUT Address *4	
Ctr	Ctr	Ctr	HCNT (pixels)	11	10	01	00	11	10	01	00	11	10	01	00	11	10	01	00	FRAME	Pixel
D18	D17	D16	register address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		Value
1	1	1	base + 0x8C	0	1	0	1	1	1	0	0	0	1	0	1	0	0	1	1	00	011
			base + 0xAC	1	0	1	0	0	0	1	1	1	0	1	0	1	1	0	0	01	011
			base + 0xCC	1	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	10	011
			base + 0xEC	0	0	1	1	1	0	1	0	1	1	0	0	1	0	1	0	11	011

310

FIG. 25

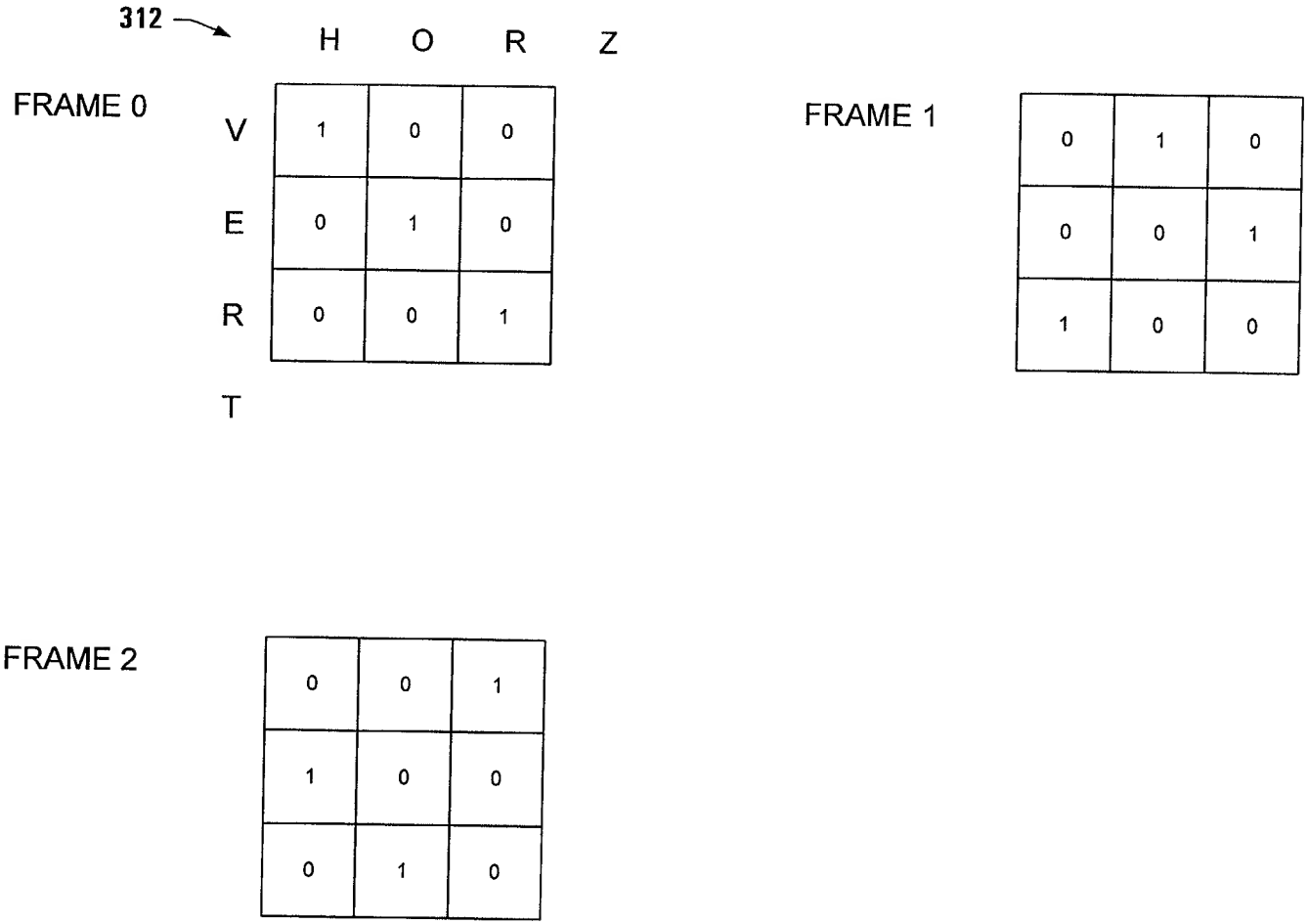
312
H O R Z
FRAME 0
V E R T
1 0 0
0 1 0
0 0 1
FRAME 1
0 1 0
0 0 1
1 0 0
FRAME 2
0 0 1
1 0 0
0 1 0

FIG. 26

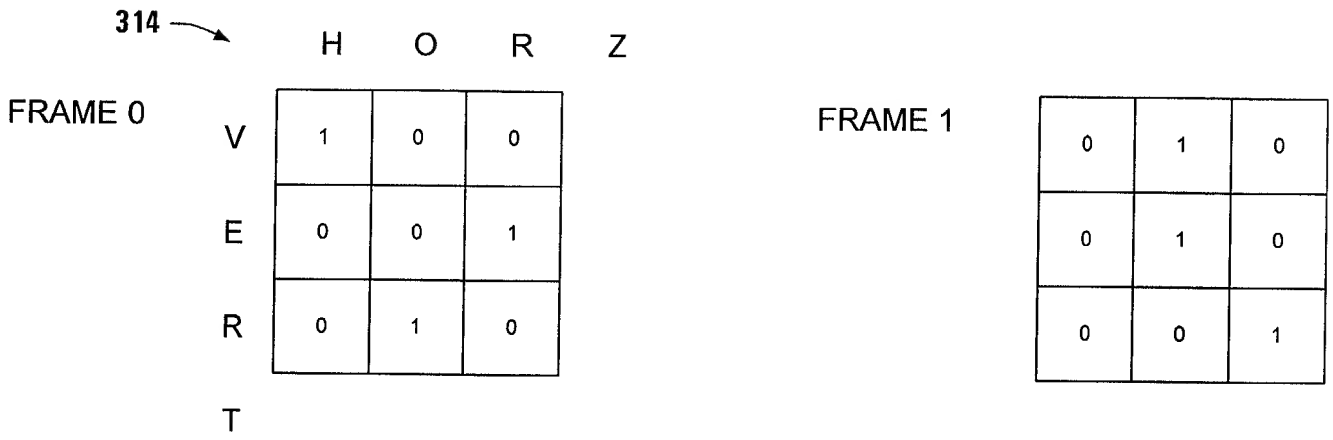
314
H
O
R
Z
FRAME 0
V
E
R
T
1
0
0
0
0
1
0
1
0
FRAME 1
0
1
0
0
1
0
0
0
1
FRAME 2
0
0
1
1
0
0
1
0
0

FIG. 27

FRAME	Vert	Horz	VCNT (lines)	11	11	11	11	10	10	10	10	01	01	01	01	00	00	00	00	GSLUT Address *4	
Ctr	Ctr	Ctr	HCNT (pixels)	11	10	01	00	11	10	01	00	11	10	01	00	11	10	01	00	FRAME	Pixel
D18	D17	D16	register address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		Value
0	0	0	base + 0x88	x	x	x	x	x	0	1	0	x	1	0	0	x	0	0	1	00	010
			base + 0xA8	x	x	x	x	x	1	0	0	x	0	1	0	x	0	1	0	01	010
			base + 0xC8	x	x	x	x	x	0	0	1	x	0	0	1	x	1	0	0	10	010
			base + 0xE8	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	11	010

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FIG. 28

PATENT APPLICATION

318

FRAME 0

	H	O	R	Z
V	1	0	0	0
E	0	0	1	1
R	0	1	0	0
T				

FRAME 1

0	1	0	0
0	1	0	0
0	0	1	1

FRAME 2

0	0	1	1
1	0	0	1
1	0	0	0

FIG. 29

FRAME	Vert	Horz	VCNT (lines)	11	11	11	11	10	10	10	10	01	01	01	01	00	00	00	00	GSLUT Address *4	
Ctr	Ctr	Ctr	HCNT (pixels)	11	10	01	00	11	10	01	00	11	10	01	00	11	10	01	00	FRAME	Pixel
D18	D17	D16	register address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		Value
0	0	0	base + 0x88	x	x	x	x	0	0	1	0	1	1	0	0	0	0	0	1	00	010
			base + 0xA8	x	x	x	x	1	1	0	0	0	0	1	0	0	0	1	0	01	010
			base + 0xC8	x	x	x	x	0	0	0	1	1	0	0	1	1	1	0	0	10	010
			base + 0xE8	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	11	010

320

FIG. 30

Display Type	Horizontal Resolution x Vertical Resolution	Video Clock frequency (MHz)	Frame Buffer Storage format	Display Data format	pixels per shift clock	Pixel Shift Clock frequency (MHz)	Vertical Frame Rate (Hz)
VFD	128 x 32	2	4 bpp	monochrome	8	0.25	400
LCD	128 x 64	2	4 bpp	monochrome	4	0.5	230
LCD	256 x 128	2	4 bpp	monochrome	4	0.5	60
"QVGA" TFT LCD	320 x 234	6.4	8 bpp	analog	1	6.4	80
QVGA STN LCD	320 x 240	4	4 bit RGB	4 bit RGB	1	4	50
HVGA STN LCD	640 x 240	8	4 bit RGB	4 bit RGB	1	8	50
"VGA" DC Plasma	640 x 400	16	4 bpp	monochrome	4	4	60
VGA EL	640 x 480	24	4 or 8 bpp	grayscale	8	3	75
VGA STN LCD	640 x 480	24	8 or 16 bpp	18 bit RGB	1	24	75
VGATFT LCD	640 x 480	24	8, 16, or 24 bpp	18 bit RGB	1	24	75
VGA CRT	640 x 480	25.175	8, 16, or 24 bpp	analog	1	NA	70
VGA CRT	640 x 480	32	8, 16, or 24 bpp	analog	1	NA	85
SVGA TFT LCD	800 x 600	40	8, 16, or 24 bpp	18 bit RGB	1	40	80
SVGA CRT	800 x 600	50	8, 16, or 24 bpp	analog	1	NA	85
XGA TFT LCD	1024 x 768	60	8, 16, or 24 bpp	18 bit RGB	2	30	72
XGA CRT	1024 x 768	75	8, 16, or 24 bpp	analog	1	NA	80
SXGA TFT LCD	1280 x 1024	85	8, 16, or 24 bpp	18 or 24 bit RGB	1	85	60
SXGA CRT	1280 x 1024	110	8, 16, or 24 bpp	analog	1	NA	70
SXGAW TFT LCD	1400 x 1024	90	8, 16, or 24 bpp	18 or 24 bit RGB	1	90	60
SXGA+ TFT LCD	1400 x 1050	110	8, 16, or 24 bpp	18 or 24 bit RGB	1	110	70
UXGA TFT LCD	1600 x 1200	135	8, 16, or 24 bpp	18 or 24 bit RGB	1	135	65
UXGA CRT	1600 x 1200	135	8, 16, or 24 bpp	analog	1	NA	60
UXGAW TFT LCD	1900 x 1200	135	8, 16, or 24 bpp	18 or 24 bit RGB	1	135	60
HDTV-2 LCD	1280 x 720	50	8, 16, or 24 bpp	24 bit RGB	1	50	50
HDTV-2 CRT	1280 x 720	66	8, 16, or 24 bpp	analog	1	NA	60
HDTV-4 LCD	1920 x 1080	135	8, 16, or 24 bpp	24 bit RGB	1	135	60
HDTV-4 CRT	1920 x 1080	135	8, 16, or 24 bpp	analog	1	NA	55
QXGA LCD	2048 x 1536	135	4 bpp	monochrome	8	16.875	40
QSXGA LCD	2560 x 2048	135	4 bpp	monochrome	8	16.875	24
QUXGA LCD	3200 x 2400	135	4 bpp	monochrome	8	16.875	17

350

FIG. 31

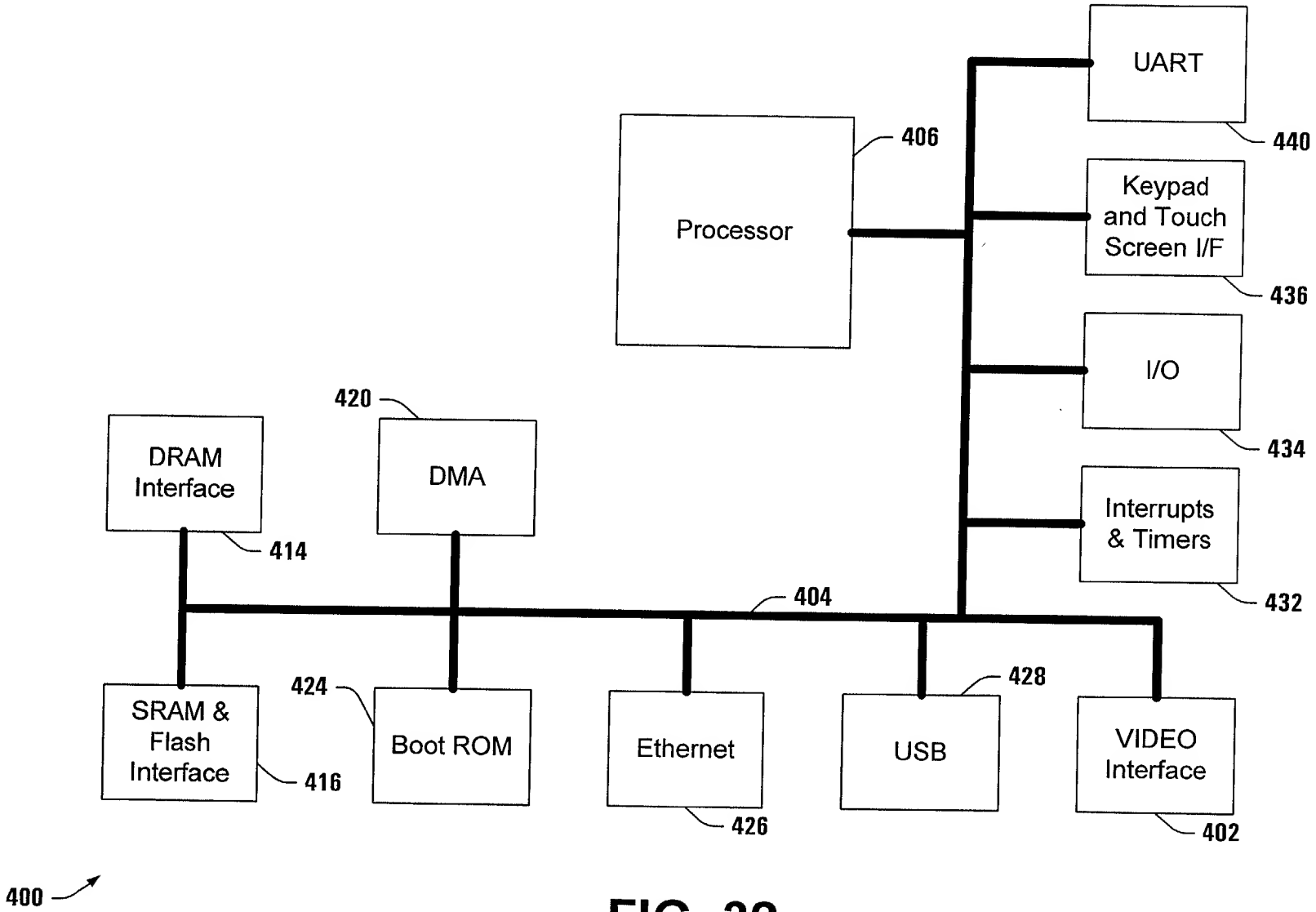
UART
440
Processor
406
Keypad and Touch Screen I/F
436
I/O
434
Interrupts & Timers
432
420
DMA
DRAM Interface
414
404
424
Boot ROM
SRAM & Flash Interface
416
Ethernet
426
428
USB
VIDEO Interface
402
400

FIG. 32

PATENT APPLICATION

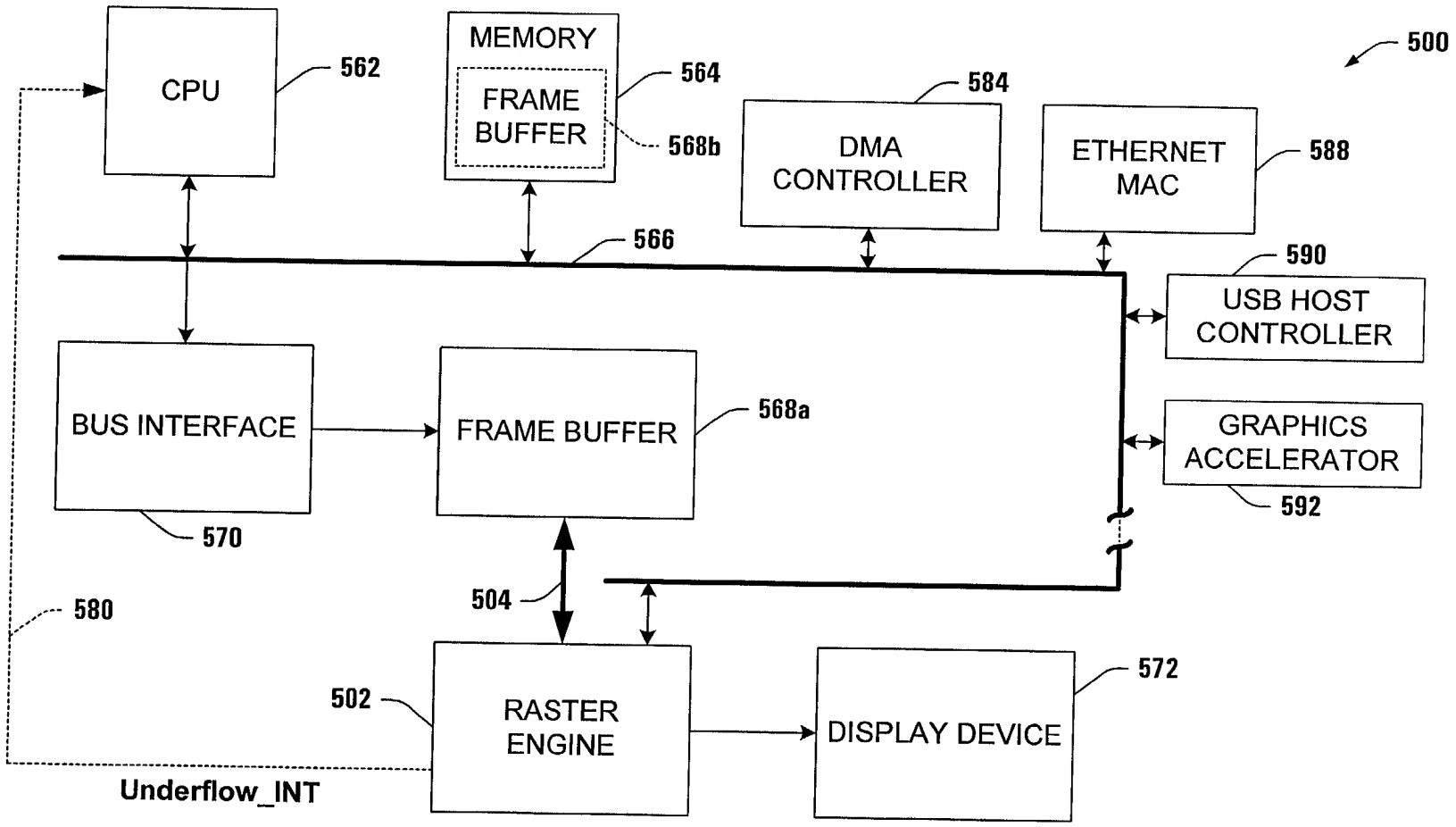

FIG. 33

PATENT APPLICATION

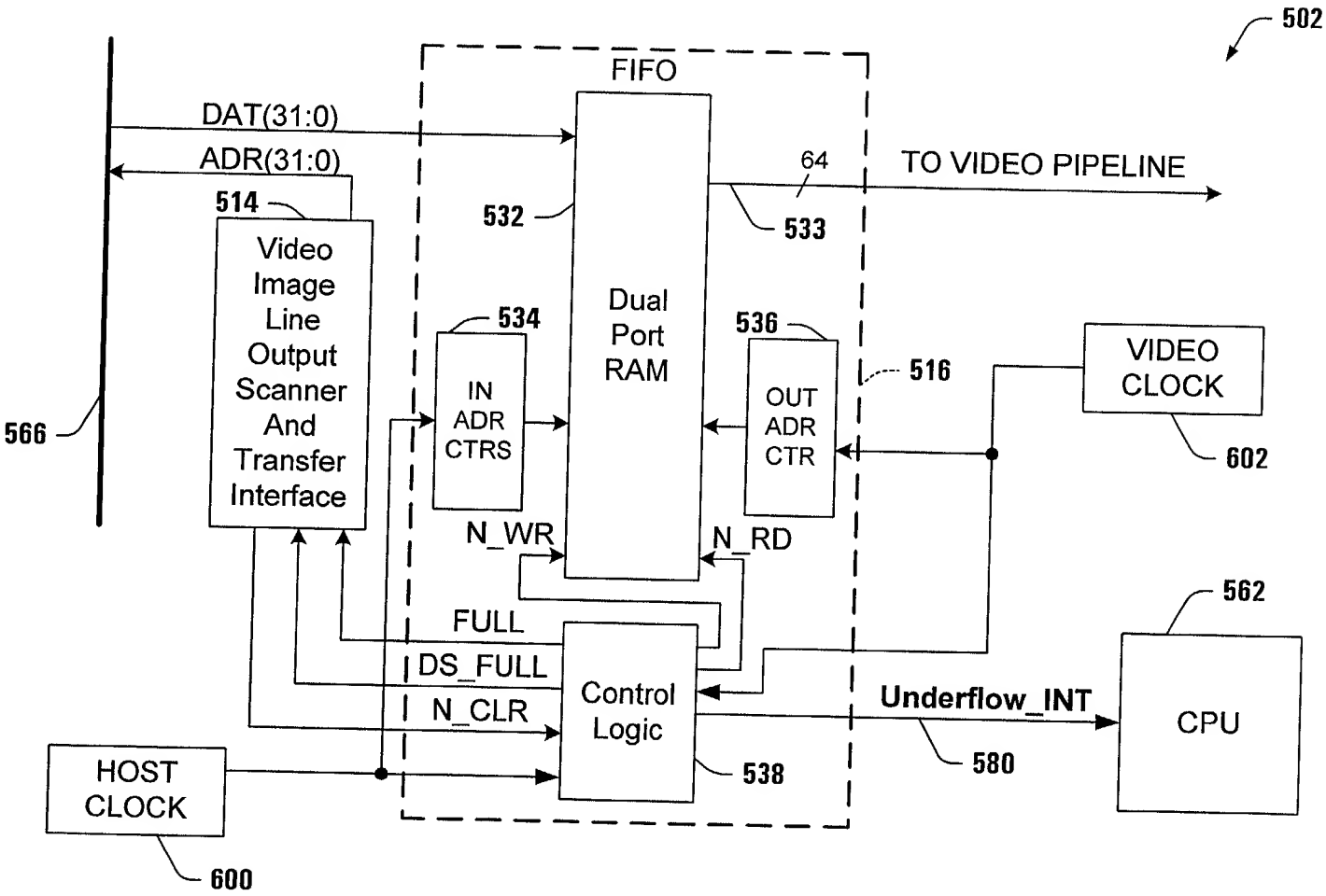

FIG. 34

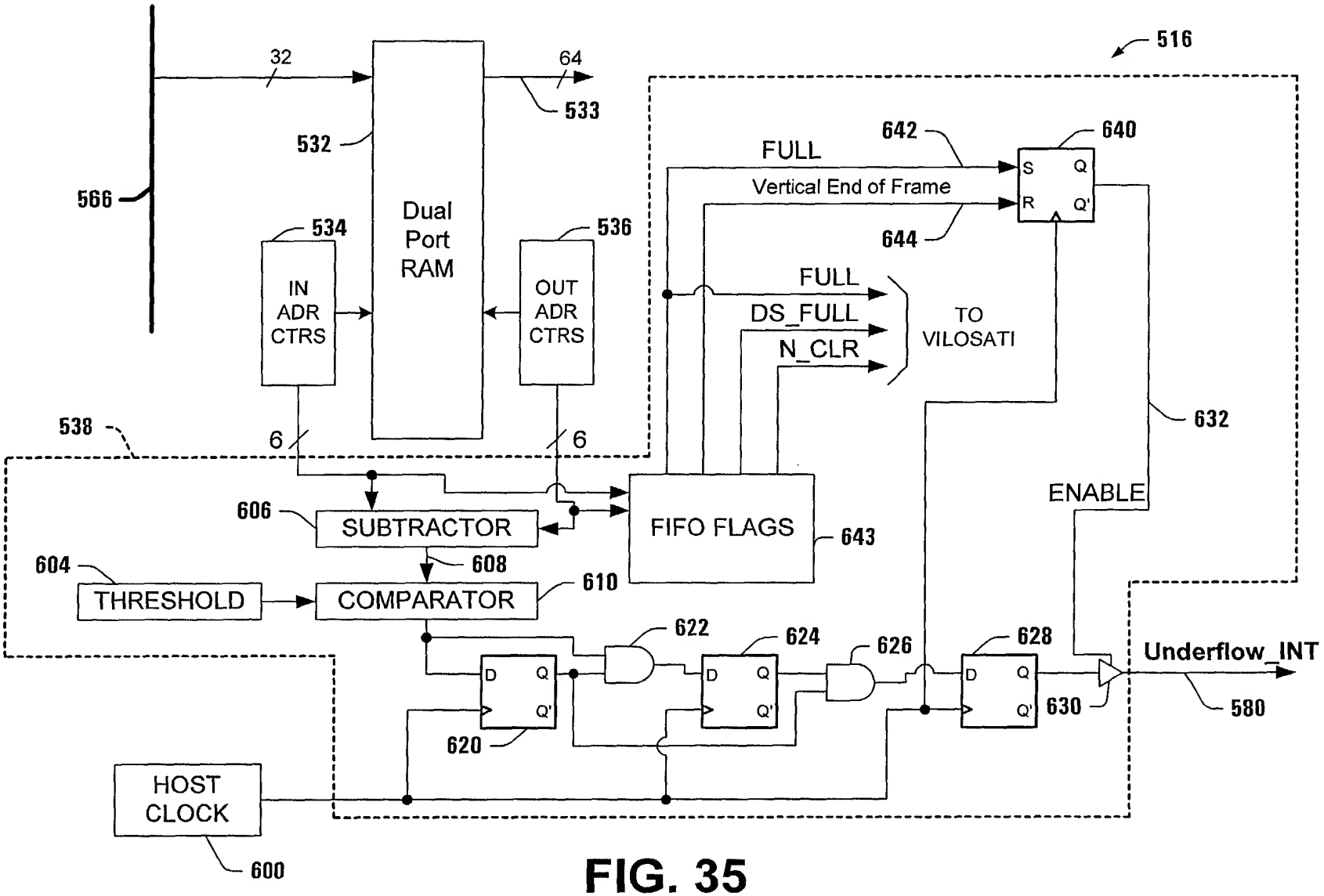
516
32
64
533
532
566
Dual Port RAM
534
IN ADR CTRS
536
OUT ADR CTRS
642
640
FULL
Vertical End of Frame
S
Q
R
Q'
644
FULL
DS_FULL
N_CLR
TO VILOSATI
632
538
6
6
606
SUBTRACTOR
FIFO FLAGS
643
ENABLE
604
608
THRESHOLD
COMPARATOR
610
622
624
626
628
Underflow_INT
D
Q
Q'
620
630
580
HOST CLOCK
600

FIG. 35

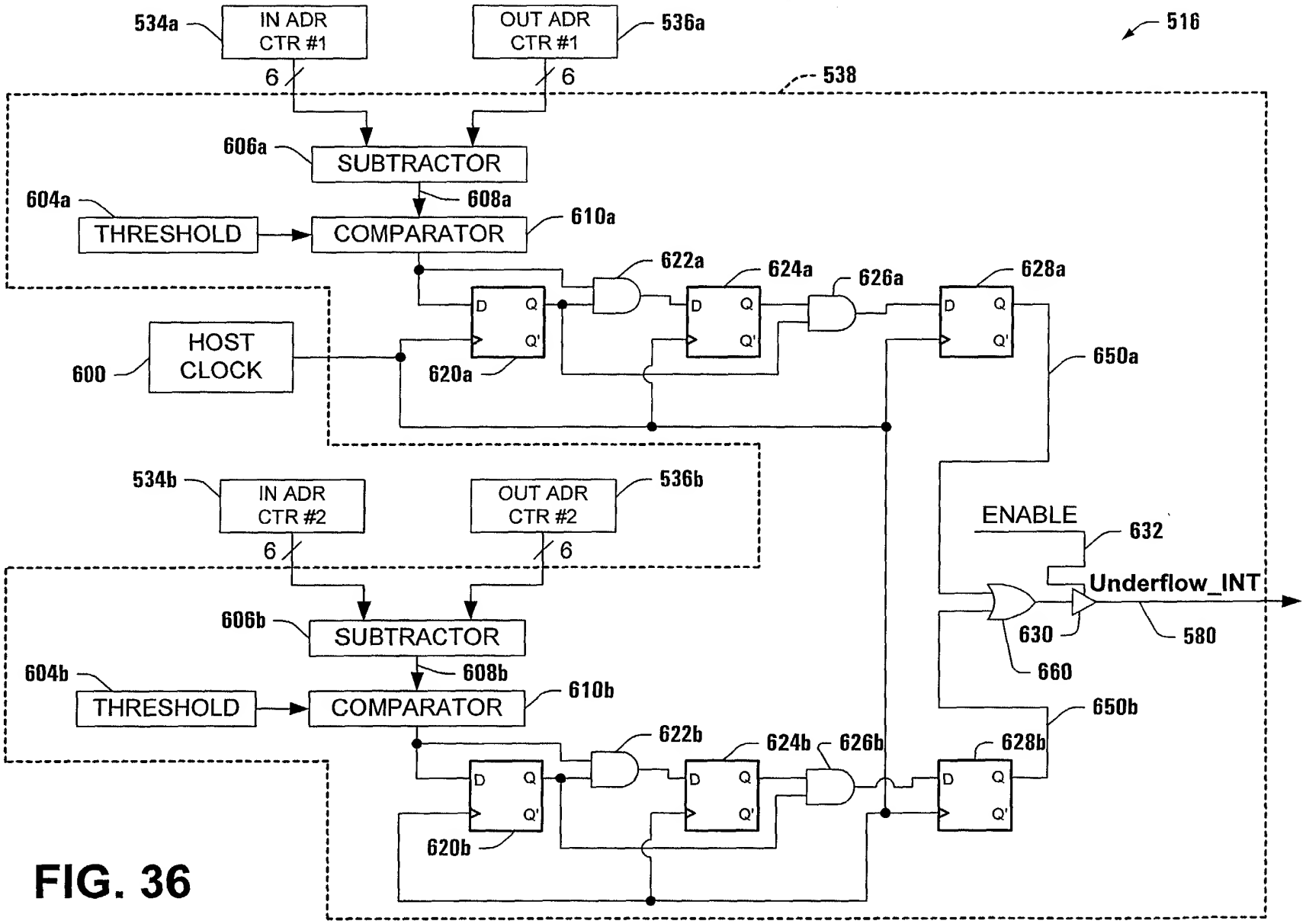
534a
IN ADR CTR #1
OUT ADR CTR #1
536a
516
538
6
6
606a
SUBTRACTOR
608a
604a
THRESHOLD
COMPARATOR
610a
622a
624a
626a
628a
D
Q
Q'
HOST CLOCK
600
620a
650a
534b
IN ADR CTR #2
OUT ADR CTR #2
536b
ENABLE
632
Underflow_INT
630
580
660
606b
SUBTRACTOR
608b
604b
THRESHOLD
COMPARATOR
610b
650b
622b
624b
626b
628b
620b

FIG. 36

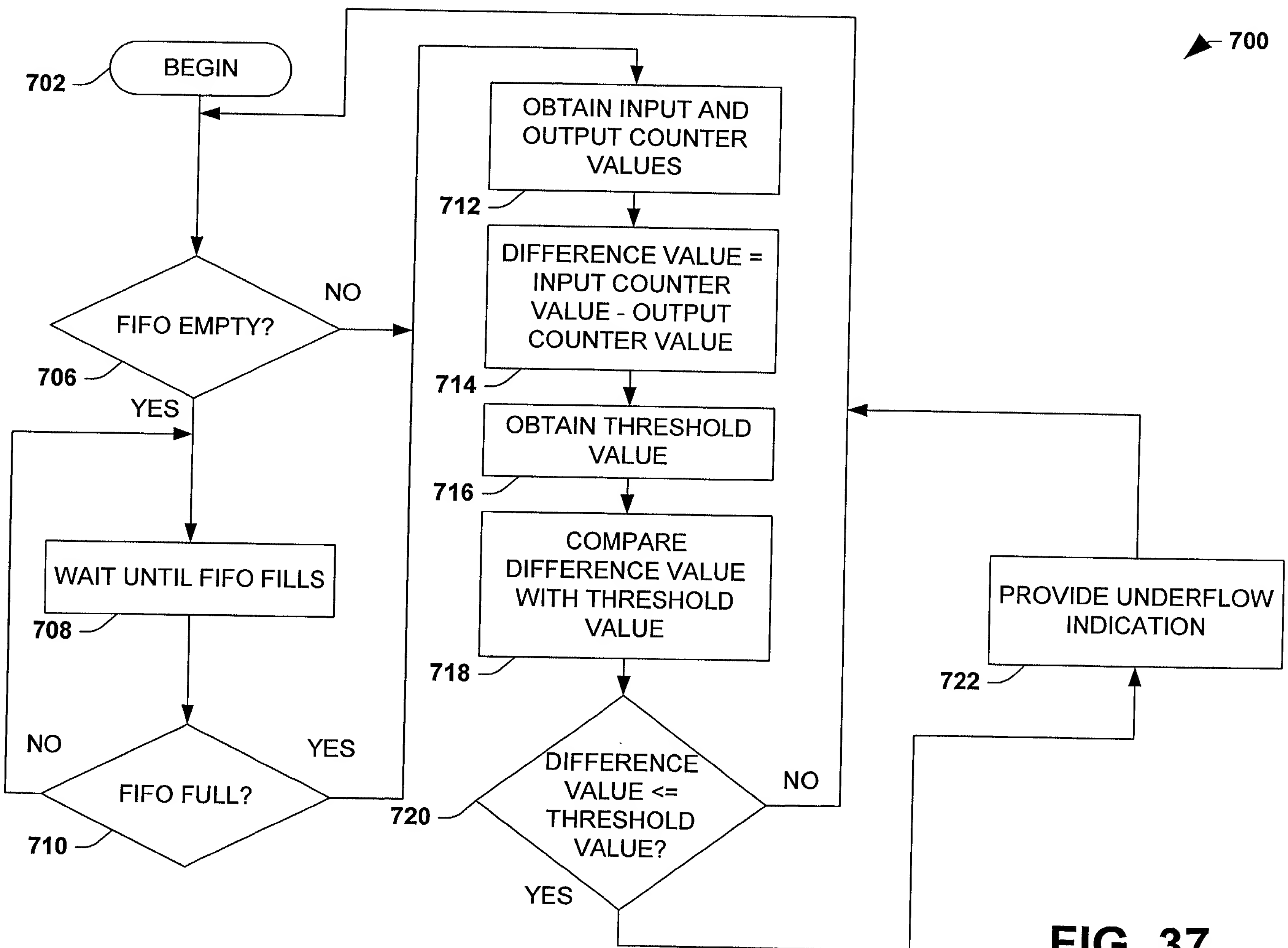
700
BEGIN
702
FIFO EMPTY?
706
NO
YES
WAIT UNTIL FIFO FILLS
708
FIFO FULL?
710
NO
YES
OBTAIN INPUT AND OUTPUT COUNTER VALUES
712
DIFFERENCE VALUE = INPUT COUNTER VALUE - OUTPUT COUNTER VALUE
714
OBTAIN THRESHOLD VALUE
716
COMPARE DIFFERENCE VALUE WITH THRESHOLD VALUE
718
DIFFERENCE VALUE <= THRESHOLD VALUE?
720
NO
YES
PROVIDE UNDERFLOW INDICATION
722

FIG. 37